High Frequency Measurement and Performance of High 'Q' Multilayer Ceramic Capacitors

Introduction

Capacitors used in High Frequency applications are generally used in two particular circuit applications:

- As a DC block providing an AC coupling path between other components.
- As a shunt path to ground for AC voltages thus providing a decoupling path.

At very high frequencies much more capacitor design data is needed by a circuit designer. As well as the normal data relating to Capacitance and Tan δ, 'Q' and E.S.R. are required. If RF/Microwave Circuit Simulation aids are being used, then the designer will require information relating to the 1 Port and 2 Port parameters, the 'S' parameters denoted by S11, S21, S12, S22.

The measurement problem becomes complex because the resultant measurements should properly describe the parameters of the multilayer capacitor but be totally uninfluenced by any test jigs used in the measurement.

The first and extensive part of this measurement sequence involves the calibration (otherwise known as "de-embedding') of all the test jigs. The information on Cal-Chip High 'Q' Capacitors contained in this catalogue has been produced utilizing a Hewlett Packard Network Analyzer - HP8753A, together with the Hewlett Packard 'S' Parameter Test Set - HP85046A.

Measurement Theory

At frequencies above 30MHz, the measurements from conventional capacitor bridges become invalid because it is not possible to maintain a true four-terminal connection to the capacitor under test, hence phase errors occur and this prohibits the separation of the resistive and reactive components which need to be measured. In addition the 'open' circuits and 'short' circuits used to calibrate the bridge become degraded. The 'open' circuits become capacitive and the 'short' circuits become inductive, hence measurement accuracy is destroyed. However, other measurement techniques can be used to solve these problems. These techniques use the behavior of electric 'waves' travelling along a transmission line, e.g. a Co-Axial Cable or a Micro-Strip Line.

If the transmission line is terminated by an unknown impedance, e.g. the capacitor under test, then a reflected wave is created which is sent back towards the Test Signal Generator and has a magnitude and phase angle dependent on the unknown impedance. We now have two waves, travelling in opposite directions, giving, in effect, the required four terminal connections to the capacitor, provided only that these waves can be separated out and independently measured.

This separation is easily possible using variations on standard Wheatstone Bridge principles. Hence by the measurement of the magnitudes and phases of three travelling waves, which are called Scattering of 'S' waves, the capacitor parameters can be calculated.

It should be noted that since these measurements rely on reflected waves, any changes in physical size, or changes in characteristic impedance between the measurement system and the points to which the capacitor is connected, will create additional and unwanted reflected waves, which will degrade the measurement accuracy.

Accuracy of capacitor placement relative to the calibration plane is also critical. For instance, measurements of a capacitor having a 'Q' of approximately 3000 and thus a Tan δ of 0.00035 will mean the phase loss angle will be of the order of 0.02 or restated -89.98 of phase or further restated, real and imaginary ratios approaching 1:3000.

To achieve measurement accuracy, the connections to the capacitor under test should operate to at least one order better than this phase angle value. In jigging or mechanical terms 1.00mm of displacement from the correct or calibration plane, represents 0.1 of phase angle, thus the phase angle errors due to the jigging etc., should be less than 0.02mm (0.0008"). These calculations assume a dielectric constant of 1 and a frequency of 100MHz.

Measurement Techniques

Three different Measurement Jig methods have been used:

- The H.P.16091A Co-Axial Test Jig was used to determine:
  - Capacitance
  - Tan δ
  - 'Q'
  - E.S.R.
- To stimulate the DC block mode and shunt or decoupling mode, special Micro-Strip Line Test Jigs were designed and made.

Equipment

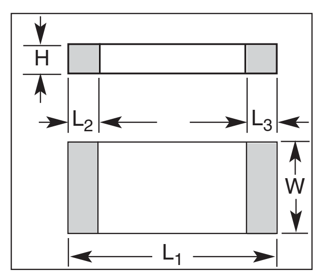
The measurement system used comprises a HP8753A Vector Network Analyzer, HP85046A 'S' Parameter Test Set and HP16091A Test Jig together with the relevant specialist cables, connectors and Micro-Strip Line Test Jigs.

Notes

1) The swept frequency range over which all measurements were taken was 1MHz to 3GHz with measurements at 10MHz increments below 1GHz, increments of 50MHz above 1 GHz.

2) For the very low capacitance values, the lowest frequencies at which sensible data was obtained appeared to be greater than 50 MHz, the data is thus presented.

3) The curves showing the resonant points for the capacitors have been left in as a guide to these points of resonance. However, due to the rapid changes in all aspects of the capacitors' parameters near to the resonant point, such measurements should be treated with caution. Above resonance the capacitance curves are dominated by the self-inductance of the capacitor.



Features:

- High 'Q' Factor at high frequencies
- High RF power capabilities
- Low ESR
- High self resonant frequencies
- Excellent stability across temperature range
- Small size

Cal-Chip Electronics, Incorporated

Surface Mount Chip Capacitors: Ultra High Frequency

General Technical Specifications

Cal-Chip Reference	Q = High Q Ceramic
Capacitance Range	0.47 pF to 1nF
Capacitance Tolerance	<10pF: ±0.1pF (B), ±0.25pF (C), ±0.5pF (D) ≥10pF: ±1% (F), ±2% (G), ±5% (J), ±10% (K), ±20% (M)
Operating Temperature Range	-55°C to +125°C
Voltage Rating	100V, 200V 500V
Environmental Classification	55/125/56
Typical Capacitance Change over Temperature Range	0 ±30ppm/°C
Measuring Frequency for Measurement of Capacitance and Dissipation Factor	1MHz
Measuring Voltage	1Vrms
Test Voltage	2.5 x nominal voltage/5 secs

Type		0603	0805	1206	1210
Dimensions					
Length (L_1)	mm	1.6±0.2	2.0±0.3	3.2±0.3	3.2±0.3
	inches	0.063±0.008	0.08±0.012	0.125±0.012	0.125±0.012
Width (W) max	mm	0.8±0.2	1.25±0.2	1.6±0.2	2.5±0.3
	inches	0.031±0.008	0.05±0.008	0.063±0.008	0.10±0.012
Thickness (H) max	mm	0.8	1.3	1.6	1.8
	inches	0.031	0.051	0.063	0.07
TerminationBand (L_2 & L_3)		Min Max	Min Max	Min Max	Min Max
	mm	0.1 0.4	0.25 0.75	0.25 0.75	0.25 0.75
	inches	0.004 0.015	0.01 0.03	0.01 0.03	0.01 0.03

Rated Voltage d.c.		0603: 100	0805: 100	0805: 200	1206: 100	1206: 200	1206: 500	1210: 100	1210: 200	1210: 500
Cap. Range	Code	Minimum and Maximum capacitance values available								
0.47pf	0R47									
0.56	0R56									
0.68	0R68									
0.82	0R82									
1.0	1R0									
1.2	1R2									
1.5	1R5									
1.8	1R8									
2.2	2R2									
2.7	2R7									
3.3	3R3									
3.9	3R9									
4.7	4R7									
5.6	5R6									
6.8	6R8									
8.2	8R2									
10	100									
12	120									
15	150									
18	180									
22	220									
27	270									
33	330									
39	390									
47	470									
56	560									
68	680									
82	820									
100	101									
120	121									
150	151									
180	181									
220	221									
270	271									
330	331									
390	391									
470	471									
560	561									
680	681									
820	821									
1.0nF	102									

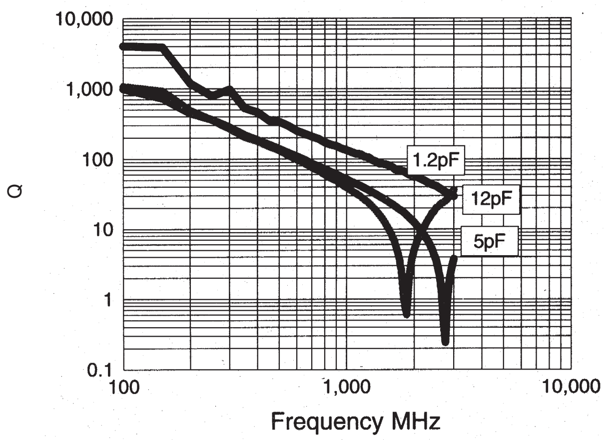
Ordering Information

Example:

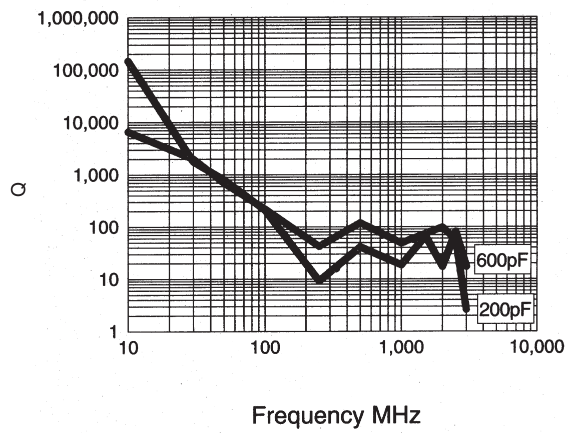
CHQ 0805 J 100 0101 K Q T

- CHQ — Chip Size
- 0805 — Type No/ Size Ref
- J — Termination Options: J = Nickel Barrier
- 100 — Voltage d.c.: 100 = 100V, 200 = 200V, 500 = 500V
- 0101 — Capacitance
- K — Capacitance Tolerance Code
- Q — Dielectric Code: Q = High Q Ceramic
- T — Packaging: T = Tape & Reel 178mm (7") dia. reel

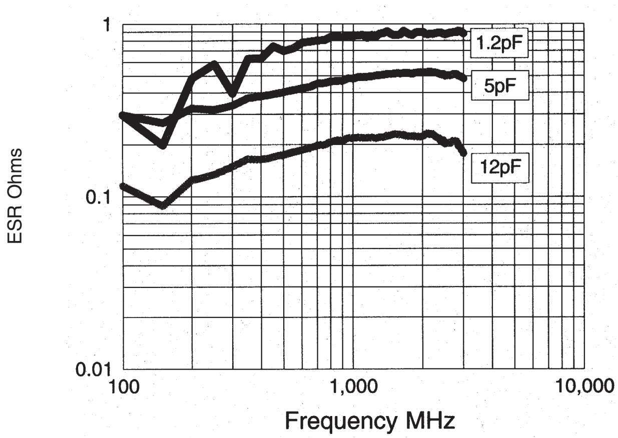
Q Chip Size - 0603 - All Values



Q Chip Size - 1210 - All Values



ESR



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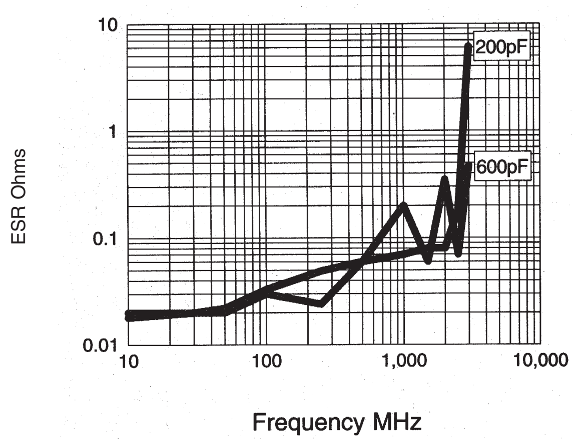

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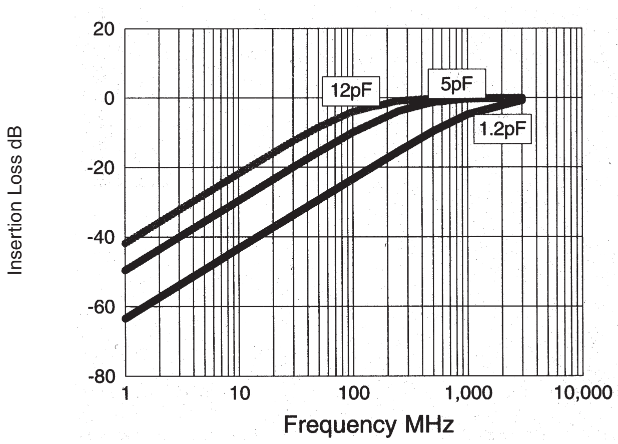

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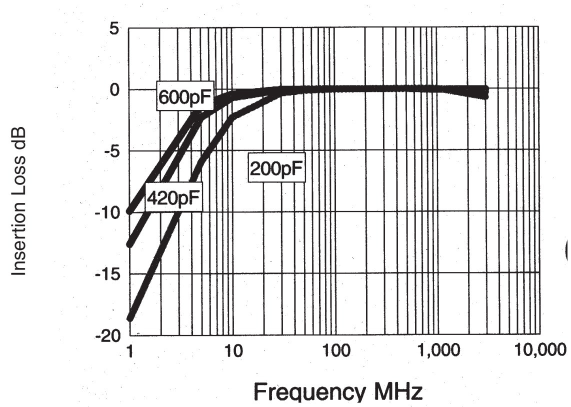
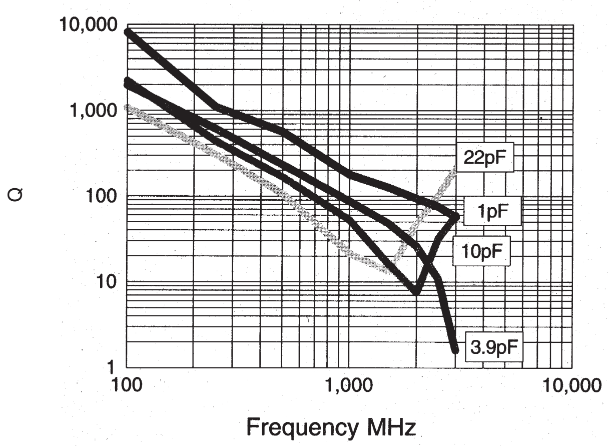


Chip Size - 0805

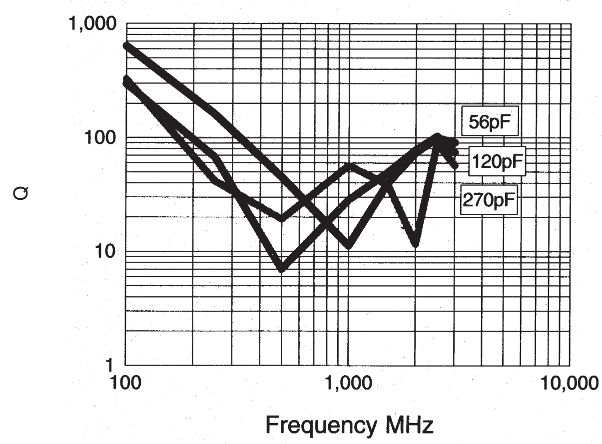
Low Values

Q

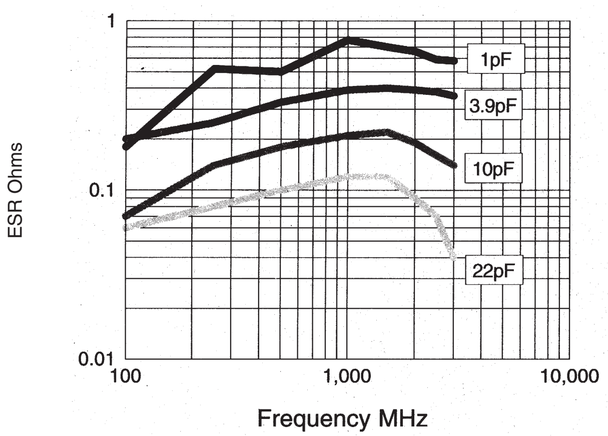


High Values

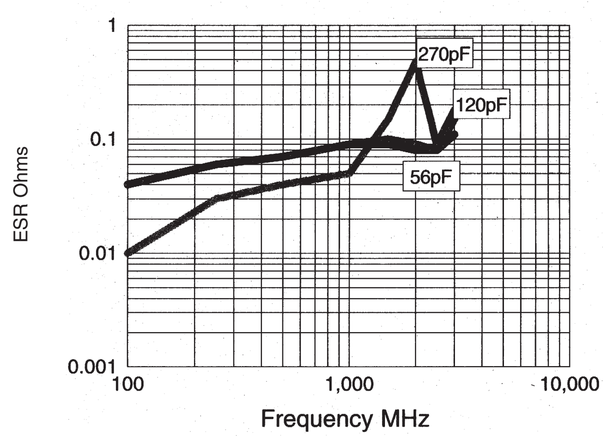
Q



ESR



ESR



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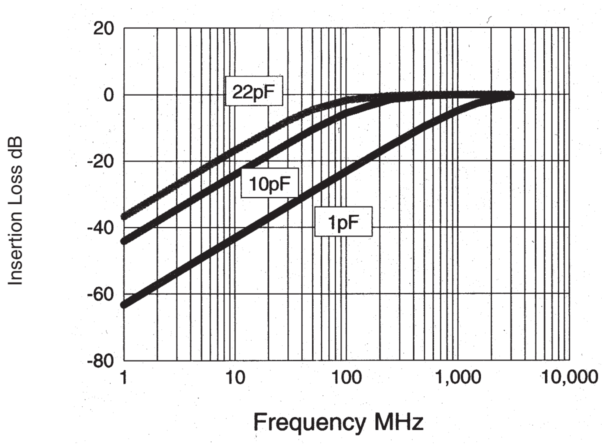

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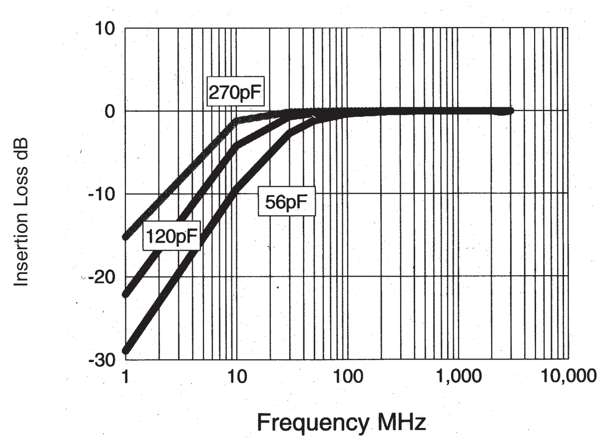
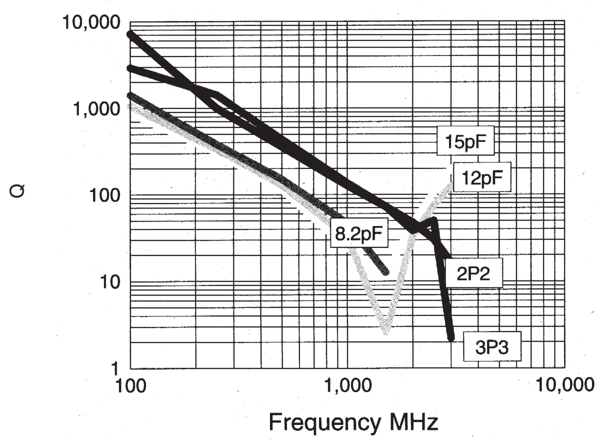


Surface Mount Chip Capacitors: Ultra High Frequency

Chip Size - 1206

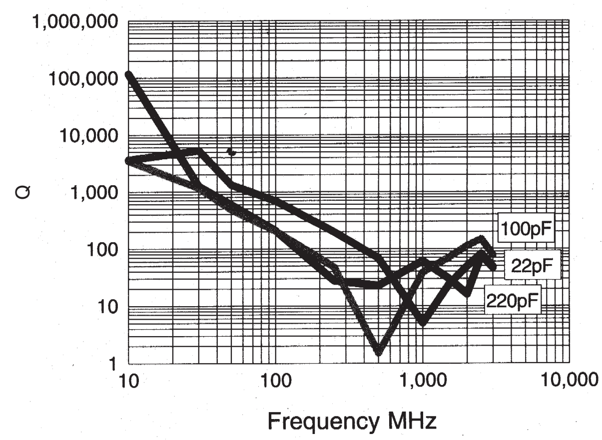
Low Values

Q

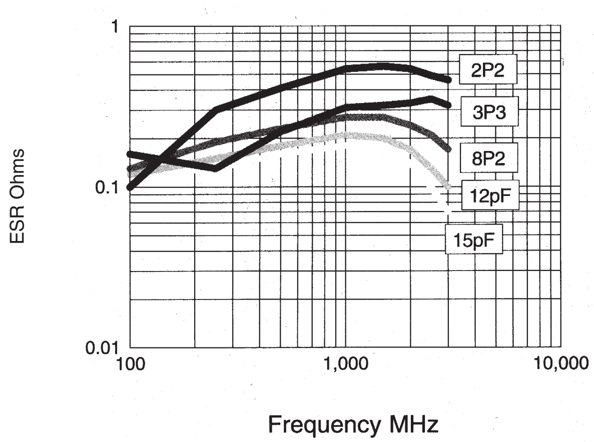


High Values

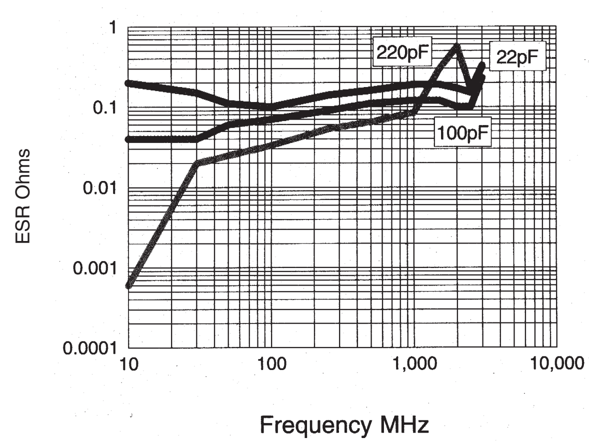
Q



ESR



ESR



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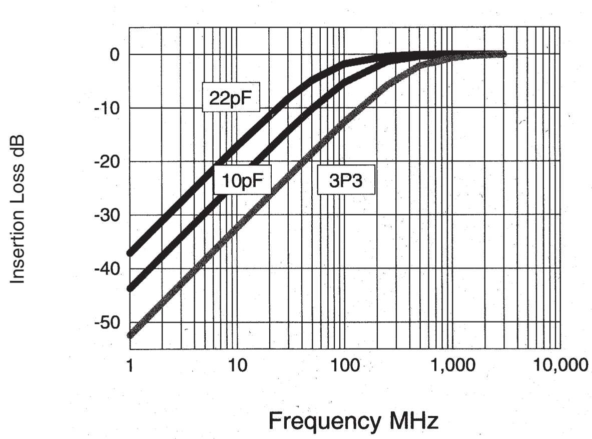

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